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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/468,015	12/20/1999	DIETMAR EGGERT	F71989US	3122

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EXAMINER	
HUYNH, KIM NGOC	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/468,015	EGGERT ET AL.	
	Examiner	Art Unit	
	Kim Huynh	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 under Waga and/or Lee have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kleveland et al. (US 5,969,929) in view of Ling (US 5,576,680).

Claim Rejections - 35 USC § 102

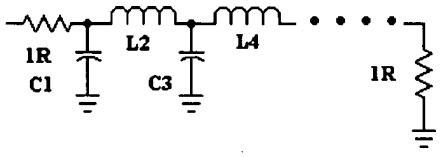
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 21-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Kleveland (US 5,969,929), provided to applicant in earlier Office Action.

Kleveland discloses (see at least Figs. 2 and 5-7) an ESD protection network having an inductor (transmission line, metal layer 231, col. 3, ll. 35-36, bondwire 514, signal trace 622 or spiral conductor 720 of Figs. 4-6) connected to a plurality of ESD clamp devices (at least 237-238, 518-520, 618-619, and 718-719) at each turn of the

inductor, wherein each ESD device having parasitic capacitance (inherent in ESD devices, col. 1, ll. 35-59) to form a low pass filter (see the equivalent circuit of Fig. 2A).



Kleveland also discloses that the inductor and ESD devices are formed on a substrate/die (239, see also col. 7, ll. 14-16 and 36-43) and the device is a semiconductor deivce.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kleveland in view of Ling (US 5,576,680).

Kleveland discloses the ESD network as discussed above, Kleveland also discloses a via 235-236 connected to each of the ESD devices 237-238 (see Fig. 2B). Kleveland does not disclose each of the turn is form on a separate layer of the integrated circuit.

Ling discloses several processes of fabricating inductive circuit on IC where Fig 4A shows a process for forming the inductive circuit 400 by connecting a plurality of

inductive coil having plurality of turns (410-410) formed on different horizontal planes of an IC chip connected by via lines 440s (col. 7, l. 59 to col. 8, l. 62). It would have been obvious to one having ordinary skill in the art to utilize the process taught by Ling in fabricating the inductor of Kleveland in order to incorporate the conventional layer-oriented process of IC fabrication technology into the "non-planar configuration" of a typical continuous spiral shape of inductive circuits (Ling, col. 1, ll. 18-51) . Please note Kleveland also discusses using conventional CMOS processes to fabricate his ESD networks (col. 7, ll. 38-42) and the advantage of combining conductive circuit with ESD protection devices (col. 1, l. 13 to col. 2, l. 38).

As for the shape of the coil and the type of metal, these are unremarkable and conventional modifications of inductive circuits and CMOS fabrication process which are within the ability of one having the ordinary skill in the art as matter of choice as discussed by Kleveland and Ling.

Response to Arguments

6. Applicant's arguments filed 10/22/04 have been fully considered but they are not persuasive.

a. Applicant argues that Kleveland is directed towards reducing parasitic capacitance of ESD protection circuit to reduce data transmissions errors in high frequency devices and therefore does not function as a "low pass filter". The examiner respectfully disagrees with this argument.

Referring to applicant's own disclosure, page 2 where applicant admits that all ESD device includes significant amount of parasitic capacitance which might degrade

the high frequency signal of I/O devices and impair proper performance of high frequency signals (p. 2, ll. 10-24). The claimed invention utilizes an inductor in series with the parasitic capacitance of the ESD device to filter out the shunt capacitance of the ESD clamp devices (p. 4, ll. 3-5) to protect high frequency signal.

Kleveland provided the *identical structure set forth in the claims 1-3 wherein an inductor is connected in series with the ESD device in a low pass RC filter configuration and using the capacitance of the ESD device as part of the transmission line to provide high bandwidth signal path and protects at low frequencies* (col. 3, ll. 56-58 and col. 5, ll. 21-30).

It is unclear how the claimed invention is distinguished by Kleveland and which limitation of the claimed invention the applicant intends to argue that is not covered by Kleveland.

b. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In this case, as pointed out in the last office action, Kleveland discusses using conventional CMOS processes to fabricate his ESD networks (col. 7, ll. 38-42) and the

advantage of combining conductive circuit with ESD protection devices (col. 1, l. 13 to col. 2, l. 38). Ling discloses several processes of fabricating inductive circuit on IC where Fig 4A shows a process for forming the inductive circuit 400 by connecting a plurality of inductive coil having plurality of turns (410-410) formed on different horizontal planes of an IC chip connected by via lines 440s (col. 7, l. 59 to col. 8, l. 62). It is obvious for one having ordinary skill in the art to look to the fabricating techniques as disclosed in Ling in order to fulfill the need of fabricating the integrated circuit of Kleveland.

Conclusion

7. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571) 272-4147.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kim Huynh
Primary Examiner
Art Unit 2182

KH
11/30/04